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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY AND METHOD OF MANUFACTURING THEREOF**

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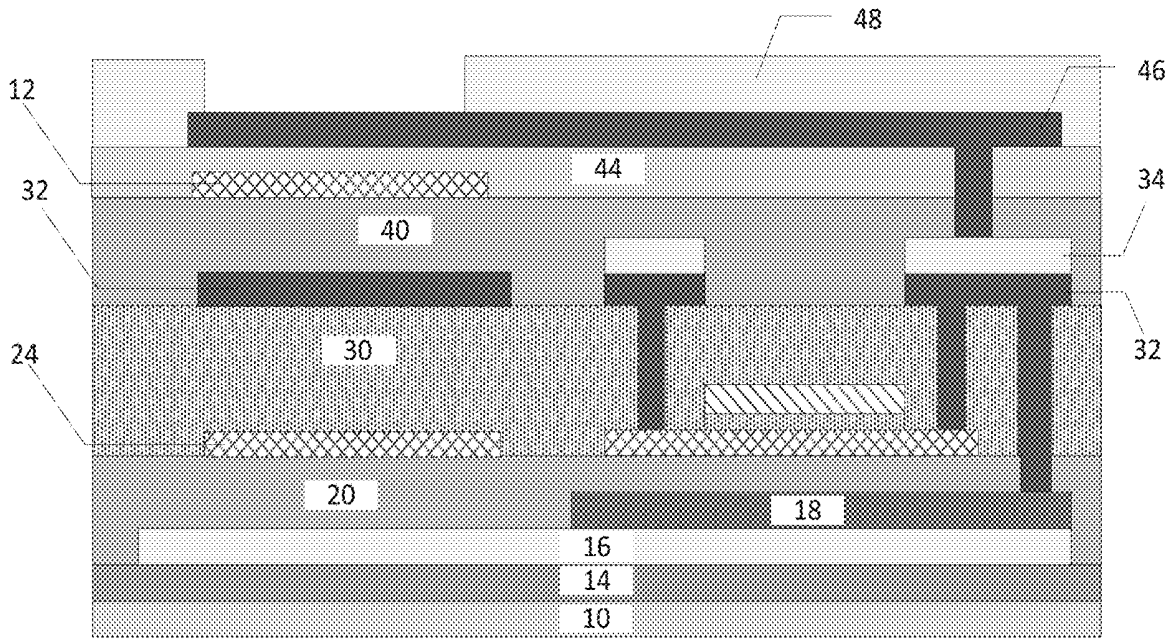
(57) **ABSTRACT**

An organic light emitting diode (OLED) display panel and a method of manufacturing thereof are provided. The display panel includes: a substrate including a color film layer and a first transparent conductive layer; the first transparent conductive layer including a first region and a second region; an active region including a first active region and a second active region, the first active region is disposed above the first region, and the second active region is disposed above the second region; a gate lamination layer, an interlayer dielectric layer, a second transparent conductive layer, a planarization layer, an anode and a pixel defining layer disposed on the second active region.



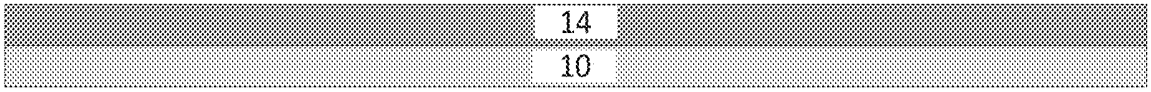


FIG. 1

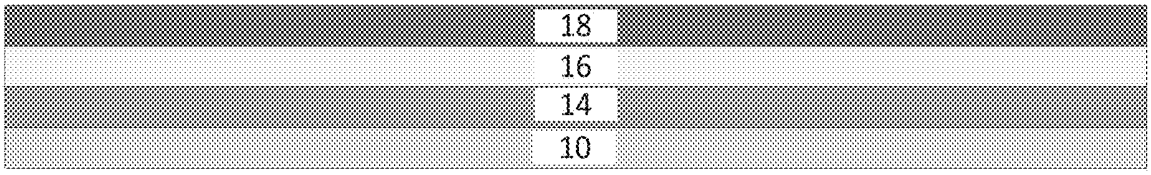


FIG. 2

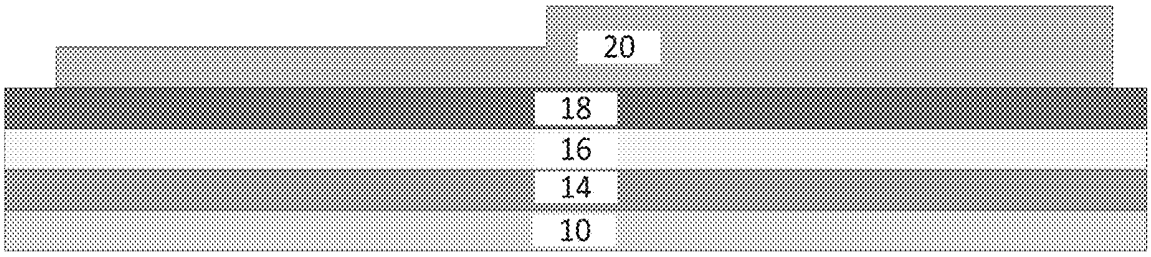


FIG. 3

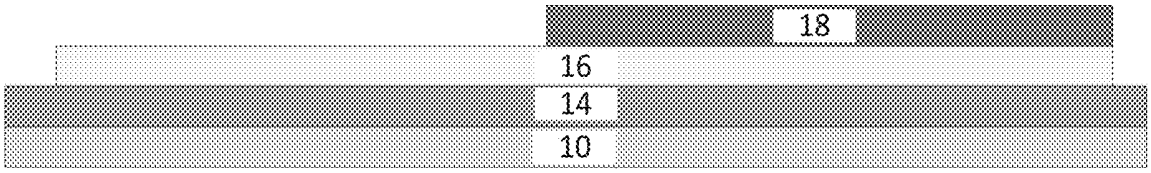


FIG. 4

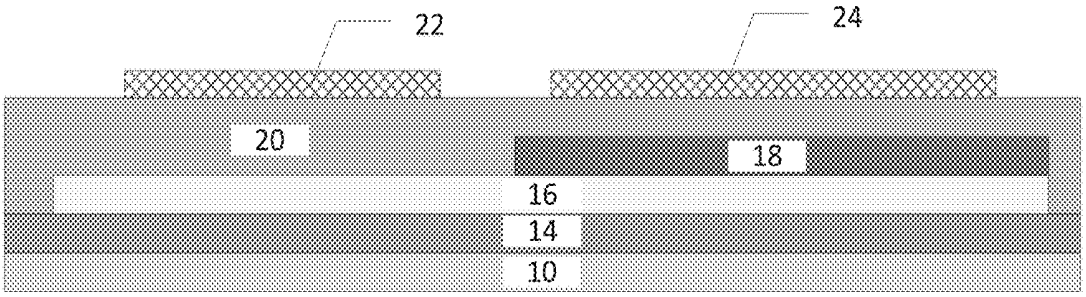


FIG. 5

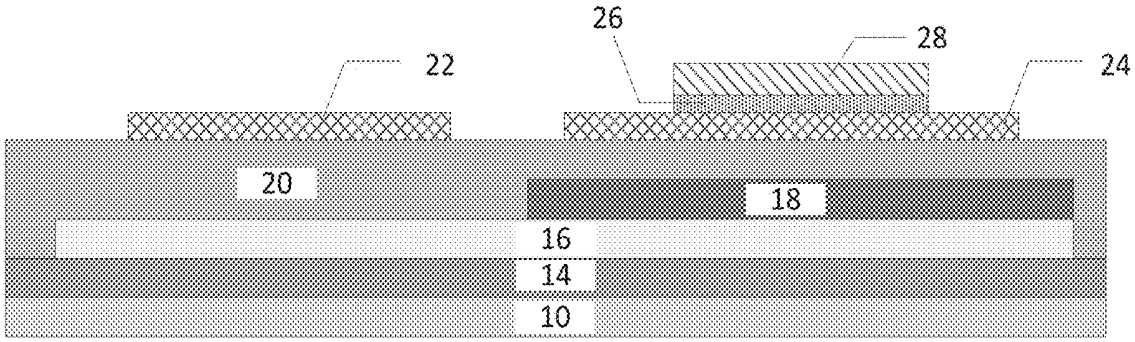


FIG. 6

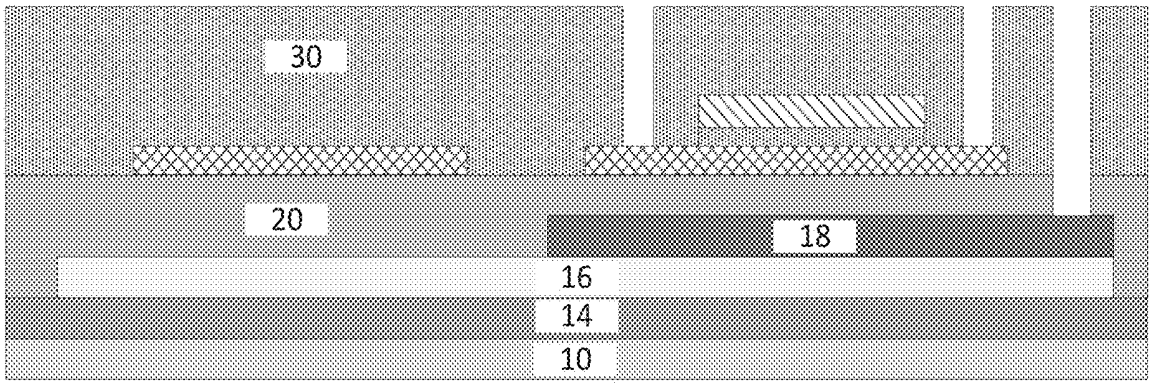


FIG. 7

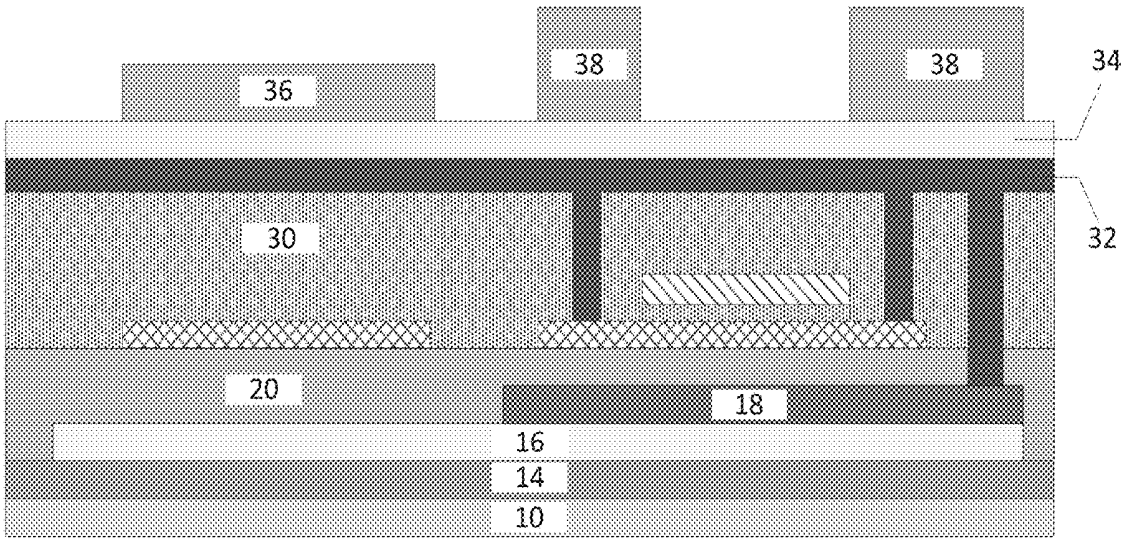


FIG. 8

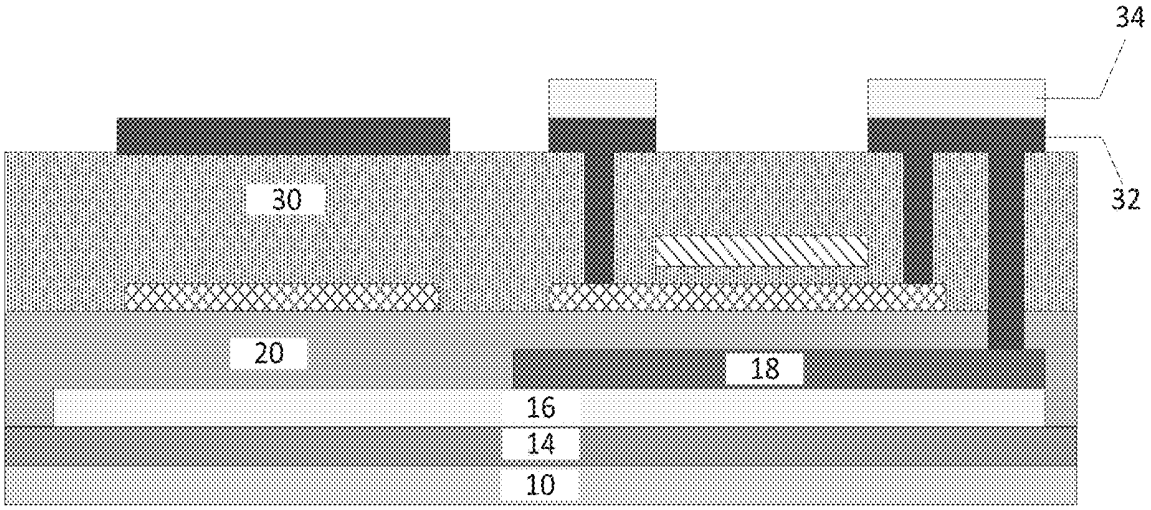


FIG. 9

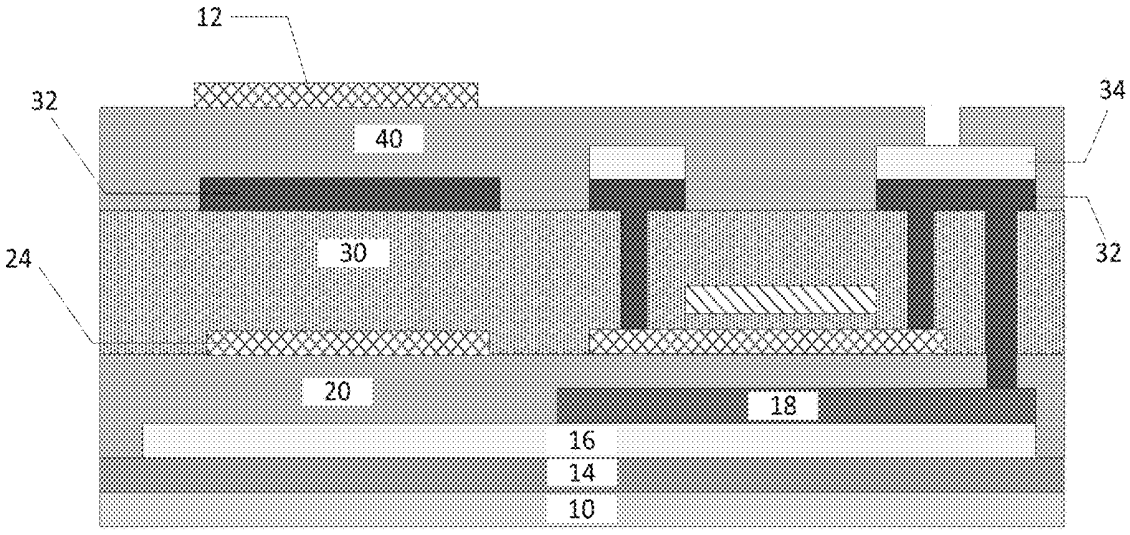


FIG. 10

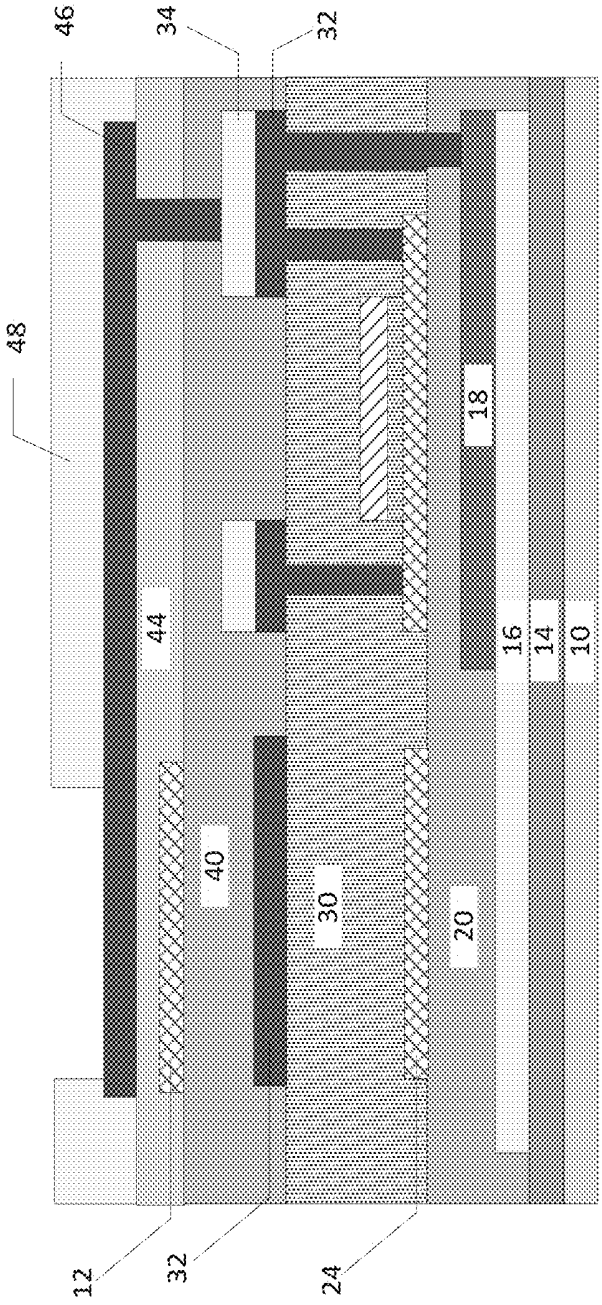


FIG. 11

ORGANIC LIGHT EMITTING DIODE DISPLAY AND METHOD OF MANUFACTURING THEREOF

BACKGROUND OF APPLICATION

Field of Application

[0001] The present application relates to the field of display technologies, and in particular, to an organic light emitting diode (OLED) display and a method for manufacturing thereof.

Description of Prior Art

[0002] With the development of display technology, the organic light emitting diode (OLED) displays have made significant progress. OLED products have attracted more and more attention and application due to their advantages, such as light weight, fast response times, wide viewing angles, high contrast, and flexibility. OLED products are mainly used in mobile phones, tablets, TVs, and other display technology fields.

Technical Problem

[0003] As panels increases in size, resistance of signal lines becomes non-negligible, resulting in an increase in a voltage drop phenomenon which leads to uneven brightness of the display panels and restricts the mass production of large-sized OLED display panels. Therefore, there is an urgent need to solve this problem.

SUMMARY OF APPLICATION

[0004] The application provides an organic light emitting diode (OLED) display panel and a manufacturing method thereof to increase the capacitance of the OLED panel.

[0005] To solve the above problems, the present application provides an OLED display panel including:

[0006] a substrate;

[0007] a first transparent conductive layer disposed on the substrate, the first transparent conductive layer including a first region and a second region; the first region corresponding to a region for forming a color film layer and the second region corresponding to a region for forming a gate lamination layer;

[0008] a first buffer layer covering the first transparent conductive layer;

[0009] an active region disposed on the first buffer layer;

[0010] the gate lamination layer disposed on the active region;

[0011] an interlayer dielectric layer covering the first buffer layer, the active region, and the gate lamination layer, the interlayer dielectric layer having a plurality of via holes;

[0012] a second transparent conductive layer disposed on the interlayer dielectric layer, wherein the second transparent conductive layer covers the active region, and realizes electrical connections of source and drain regions through the via holes;

[0013] a planarization layer covering the interlayer dielectric layer and the second transparent conductive layer;

[0014] the color film layer disposed on the planarization layer, the color film layer is disposed on the first region;

[0015] a second buffer layer covering the color film layer and the planarization layer;

[0016] an anode disposed on the second buffer layer;

[0017] a pixel defining layer exposing the anode; and

[0018] a light emitting structure covering the pixel defining layer and the anode; wherein

[0019] the active region includes a first active region and a second active region, the first active region is disposed above the first region and the second active region is disposed above the second region.

[0020] According to one aspect of the application, a projection of the color film layer on a horizontal plane, a projection of the first region on a horizontal plane, and a projection of the first active region on a horizontal plane overlap.

[0021] According to one aspect of the application, the display panel further includes a light shielding metal layer between the first transparent conductive layer and the first buffer layer, a projection of the light shielding metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

[0022] According to one aspect of the application, the display panel further includes a metal layer disposed on the second transparent conductive layer, a projection of the metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

[0023] According to one aspect of the application, material forming the metal layer is a light shielding metal.

[0024] The present application provides an OLED display panel, including:

[0025] a substrate;

[0026] a first transparent conductive layer disposed on the substrate, the first transparent conductive layer including a first region and a second region; the first region corresponding to a region for forming a color film layer and the second region corresponding to a region for forming a gate lamination layer;

[0027] a first buffer layer covering the first transparent conductive layer;

[0028] an active region disposed on the first buffer layer;

[0029] the gate lamination layer disposed on the active region;

[0030] an interlayer dielectric layer covering the first buffer layer, the active region, and the gate lamination layer, the interlayer dielectric layer having a plurality of via holes;

[0031] a second transparent conductive layer disposed on the interlayer dielectric layer, wherein the second transparent conductive layer covers the active region, and realizes electrical connections of source and drain regions through the via holes;

[0032] a planarization layer covering the interlayer dielectric layer and the second transparent conductive layer;

[0033] the color film layer disposed on the planarization layer, the color film layer is disposed on the first region;

[0034] a second buffer layer covering the color film layer and the planarization layer;

[0035] an anode disposed on the second buffer layer;

[0036] a pixel defining layer exposing the anode; and

[0037] a light emitting structure covering the pixel defining layer and the anode.

[0038] According to one aspect of the application, the active region includes a first active region and a second active region, the first active region is disposed above the first region and the second active region is disposed above the second region.

[0039] According to one aspect of the application, a projection of the color film layer disposed on a horizontal plane,

a projection of the first region disposed on a horizontal plane, and a projection of the first active region disposed on a horizontal plane overlap.

[0040] According to one aspect of the application, the display panel further includes a light shielding metal layer between the first transparent conductive layer and the first buffer layer, a projection of the light shielding metal layer disposed on a horizontal plane overlaps with a projection of the second active region disposed on a horizontal plane.

[0041] According to one aspect of the application, the display panel further includes a metal layer disposed on the second transparent conductive layer, a projection of the metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

[0042] According to one aspect of the application, the material forming the metal layer is a light shielding metal.

[0043] The present application further provides a method of manufacturing an OLED display panel, including the steps of:

[0044] providing a substrate;

[0045] forming a first transparent conductive layer disposed on the substrate, wherein the first transparent conductive layer includes a first region and a second region, the first region is used to form a color film layer, and the second region is used to form a gate lamination layer;

[0046] forming a first buffer layer covering the first transparent conductive layer;

[0047] forming an active region disposed on the first buffer layer;

[0048] forming the gate lamination layer over the active region;

[0049] forming an interlayer dielectric layer covering the first buffer layer, the active region, and the gate lamination layer, the interlayer dielectric layer having a plurality of via holes;

[0050] forming a second transparent conductive layer disposed on the interlayer dielectric layer, wherein the second transparent conductive layer is disposed above the first region and the second region, and realizes electrical connections of source and drain regions through the via holes;

[0051] forming a planarization layer covering the interlayer dielectric layer and the second transparent conductive layer;

[0052] forming the color film layer disposed on the planarization layer, the color film layer is disposed over the first region;

[0053] forming a second buffer layer covering the color film layer and the planarization layer;

[0054] forming an anode disposed on the second buffer layer;

[0055] forming a pixel defining layer exposing the anode; and

[0056] forming a light emitting structure covering the pixel defining layer and the anode.

[0057] According to one aspect of the application, the active region includes a first active region and a second active region, the first active region is disposed above the first region and the second active region is disposed above the second region.

[0058] According to one aspect of the application, a projection of the color film layer on a horizontal plane, a projection of the first region on a horizontal plane, and a projection of the first active region on a horizontal plane overlap.

[0059] According to one aspect of the application, after forming the first transparent conductive layer, the method further includes the following steps:

[0060] forming a light shielding metal layer covering the first transparent conductive layer;

[0061] patterning the light shielding metal layer, so that its projection on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

[0062] According to one aspect of the application, the method of patterning the light shielding metal layer and the first transparent conductive layer includes:

[0063] providing a mask having a first pattern for forming the first transparent conductive layer and a second pattern for forming the light shielding metal layer;

[0064] forming a photoresist covering the light shielding metal layer and the first transparent conductive layer, the photoresist having a first thickness;

[0065] the photoresist is patterned by the mask to form a first photoresist over the first transparent conductive layer and a second photoresist over the light shielding metal layer, the thickness of the first photoresist is less than the thickness of the second photoresist;

[0066] the light shielding metal layer and the first transparent conductive layer are patterned by using the first photoresist and the second photoresist as a mask.

[0067] According to one aspect of the application, the first pattern and the second pattern of the mask have different transmittances, and the transmittance of the first pattern is smaller than the transmittance of the second pattern.

[0068] According to one aspect of the application, after forming the second transparent conductive layer, the method further includes the steps of:

[0069] forming a metal layer over the second transparent conductive layer, a projection of the metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

[0070] According to one aspect of the application, the material forming the metal layer is a light shielding metal.

Beneficial Effect

[0071] The OLED display panel provided by the present application has a first transparent conductive layer disposed on the base plate, a first active region disposed on the first transparent conductive layer, and a second transparent conductive layer disposed on the first active region. The first transparent conductive layer, the first active region and the second transparent conductive layer are respectively separated by a buffer layer and an interlayer dielectric layer, thereby forming a three-layer parallel capacitor structure. The present application can effectively increase the capacitance of the display panel and eliminate the pressure drop phenomenon.

BRIEF DESCRIPTION OF DRAWINGS

[0072] In order to describe clearly the embodiment in the present disclosure or the prior art, the following will introduce the drawings for the embodiment shortly. Obviously, the following description is only a few embodiments, for the common technical personnel in the field it is easy to acquire some other drawings without creative work.

[0073] FIG. **1** to FIG. **11** are schematic structural diagrams of an organic light emitting diode (OLED) display panel in different process steps in an embodiment of the present application.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0074] Description of following embodiment, with reference to accompanying drawings, is used to exemplify specific embodiments which may be carried out in the present disclosure. Directional terms mentioned in the present disclosure, such as "top", "bottom", "front", "back", "left", "right", "inside", "outside", "side", etc., are only used with reference to orientation of the accompanying drawings. Therefore, the directional terms are intended to illustrate, but not to limit, the present disclosure. In the drawings, components having similar structures are denoted by same numerals.

[0075] The application provides an organic light emitting diode (OLED) display panel and a manufacturing method thereof to increase the capacitance of the OLED panel. The application will be described in detail below with reference to the accompanying drawings. Specifically, referring to FIG. **1** to FIG. **11**, FIG. **1** to FIG. **11** are schematic structural diagrams of an OLED display panel in different process steps in an embodiment of the present application.

[0076] As shown in FIG. **11**, the present application provides an OLED display panel including:

[0077] a substrate **10**;

[0078] a first transparent conductive layer **16** disposed on the substrate **10**, the first transparent conductive layer **16** including a first region and a second region. The first region corresponds to a region for forming a color film layer and the second region corresponds to a region for forming a gate lamination layer;

[0079] a first buffer layer **20** covering the first transparent conductive layer **16**;

[0080] an active region **24** disposed on the first buffer layer **20**. The active region **24** includes a first active region and a second active region, the first active region is disposed above the first region, and the second active region is disposed above the second region;

[0081] the gate lamination layer disposed on the active region **24**;

[0082] an interlayer dielectric layer **30** covering the first buffer layer **20**, the active region **24**, and the gate lamination layer, the interlayer dielectric layer **30** having a plurality of via holes;

[0083] a second transparent conductive layer **32** disposed on the interlayer dielectric layer **30**, wherein the second transparent conductive layer **32** covers the active region **24**, and realizes electrical connections of source and drain regions through the via holes;

[0084] a planarization layer **40** covering the interlayer dielectric layer **30** and the second transparent conductive layer **32**;

[0085] the color film layer **12** disposed on the planarization layer **40**, the color film layer **12** is disposed on the first region;

[0086] a second buffer layer **44** covering the color film layer **12** and the planarization;

[0087] an anode **46** disposed on the second buffer **44** layer;

[0088] a pixel defining layer **48** exposing the anode **46**; and

[0089] a light emitting structure covering the pixel defining layer **48** and the anode **46**.

[0090] According to one aspect of the application, a projection of the color film layer **12** disposed on a horizontal plane, a projection of the first region disposed on a horizontal plane, and a projection of the first active region **24** disposed on a horizontal plane overlap.

[0091] Preferably, the display panel further includes a light shielding metal layer **18** between the first transparent conductive layer **16** and the first buffer layer **20**, a projection of the light shielding metal layer **18** disposed on a horizontal plane overlaps with a projection of the second active region **24** disposed on a horizontal plane. Therefore, the first region of the first transparent conductive layer of the active region, the first active region, the second transparent conductive layer, the anode and the insulating layers between them constitute a plurality of capacitor structures connected in series to increase the capacitance of the OLED panel.

[0092] In the present embodiment, the display panel further includes a metal layer **34** disposed on the second transparent conductive layer **32**, a projection of the metal layer **34** on a horizontal plane overlaps with a projection of the second active region **24** on a horizontal plane. Material forming the metal layer **34** is a light shielding metal.

[0093] The light shielding metal layer **18** and the metal layer **34** can block the light emitted by the light emitting structure from entering the light sensor under the display panel. Thereby, the interference of the light of the panel in the sensor can be eliminated.

[0094] The present application further provides a method of manufacturing an OLED display panel, and the method will be described in detail below.

[0095] First, providing a substrate **10**, the substrate **10** can be a rigid substrate such as glass or a flexible substrate such as Polyimide (PI).

[0096] Preferably, after the substrate **10** is formed, the method further includes: forming a buffer layer **14** above the substrate **10** for improving an interface state between the substrate **10** and the first transparent conductive layer **16**.

[0097] After that, referring to FIG. **2**, forming the first transparent conductive layer **16** disposed on the substrate **10**, wherein the first transparent conductive layer **16** includes a first region and a second region, the first region is used to form a color film layer **12**, and the second region is used to form a gate lamination layer.

[0098] Preferably, after the transparent conductive layer **16** is formed, the method further includes: forming the light shielding metal layer **18** covering the first transparent conductive layer **16**; and then patterning the light shielding metal layer **18** to make its projection on a horizontal plane overlaps with a projection of the second active region on a horizontal plane. Thereafter, the light shielding metal layer **18** and the first transparent conductive layer **16** are patterned, as shown in FIG. **4**.

[0099] Specifically, providing a mask having a first pattern for forming the first transparent conductive layer **16** and a second pattern for forming the light shielding metal layer.

[0100] Forming a photoresist covering the light shielding metal layer and the first transparent conductive layer **16**, the photoresist having a first thickness. The photoresist is patterned by the mask to form a first photoresist over the first transparent conductive layer **16** and a second photoresist over the light shielding metal layer, the thickness of the first photoresist is less than the thickness of the second photo-

resist. The light shielding metal layer and the first transparent conductive layer **16** are patterned by using the first photoresist and the second photoresist as a mask, as shown in FIG. **3**.

[0101] In the present embodiment, the first pattern and the second pattern of the mask have different transmittance, and the transmittance of the first pattern is smaller than the transmittance of the second pattern. Specifically, it is implemented here by a half tone mask process. Wherein, the first pattern and the second pattern of the mask have different transmittances, and the transmittance of the first pattern is smaller than the transmittance of the second pattern. In practice, the transmittances of the first pattern and the second pattern are adjusted according to the thickness requirements of the photoresist. The half tone mask technology is a conventional technical means in the art and will not be described here.

[0102] After that, referring to FIG. **5**, forming a first buffer layer **20** covering the first transparent conductive layer **16**, and forming an active region **24** disposed on the buffer layer **20**. Wherein the active region **24** includes a first active region and a second active region, the first active region is disposed above the first region, and the second active region is disposed above the second region.

[0103] After that, referring to FIG. **6**, forming the gate lamination layer over the active region **24**. The gate lamination layer includes a gate dielectric layer **26** and a metal layer **28** in order from bottom to top.

[0104] After that, referring to FIG. **7**, forming an interlayer dielectric layer **30** covering the second buffer layer **20**, the first active region, and the gate lamination layer, the interlayer dielectric layer **30** having a plurality of via holes. Specifically, the via holes includes a first via hole exposing the source, a second via hole exposing a drain, and a third via hole exposing the entire metal layer **18**.

[0105] After that, referring to FIG. **8**, forming a second transparent conductive layer **32** disposed on the interlayer dielectric layer **30**, wherein the second transparent conductive layer **32** is disposed above the first region and the second region, and realizes electrical connections of source and drain regions through the via holes.

[0106] Preferably, referring to FIG. **8**, after forming the second transparent conductive layer **32**, the method further includes the steps of: forming a metal layer **34** over the second transparent conductive layer **32**, a projection of the metal layer **34** on a horizontal plane overlaps with a projection of the second active region on a horizontal plane. The material forming the metal layer **34** is a light shielding metal, as shown in FIG. **9**.

[0107] Thereafter, as shown in FIG. **10**, the planarization layer **40** covering the interlayer dielectric layer **30** and the second transparent conductive layer **32**, the color film layer **12** disposed on the planarization layer **40** are formed. The color film layer **12** is disposed above the first region. The color film layer **12** is composed of a regular arrangement of color films of red, green and blue colors. A projection of the color film layer **12** on a horizontal plane, a projection of the first region on a horizontal plane, and a projection of the first active region on a horizontal plane overlap.

[0108] Thereafter, as shown in FIG. **11**, a second buffer layer **44** covering the color film layer **12** and the planarization layer **40**, an anode **46** disposed above the second buffer layer **44** and an pixel definition layer **48** exposing the anode **46** are formed. Finally, an OLED display panel as shown in FIG. **11** is formed.

[0109] The OLED display panel provided by the present application has a first transparent conductive layer **16** disposed on the base plate, a first active region **24** disposed on the first transparent conductive layer **16**, and a second transparent conductive layer **32** disposed on the first active region **24**. The first transparent conductive layer **16**, the first active region **24** and the second transparent conductive layer **32** are respectively separated by a buffer layer and an interlayer dielectric layer **30**, thereby forming a three-layer parallel capacitor structure. The present application can effectively increase the capacitance of the display panel and eliminate the pressure drop phenomenon.

[0110] As is understood by persons skilled in the art, the foregoing preferred embodiments of the present disclosure are illustrative rather than limiting of the present disclosure. It is intended that they cover various modifications and that similar arrangements be included in the spirit and scope of the present disclosure, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. An organic light emitting diode (OLED) display panel comprising:

a substrate;

a first transparent conductive layer disposed on the substrate, the first transparent conductive layer comprising a first region and a second region; the first region corresponding to a region for forming a color film layer and the second region corresponding to a region for forming a gate lamination layer;

a first buffer layer covering the first transparent conductive layer;

an active region disposed on the first buffer layer;

the gate lamination layer disposed on the active region;

an interlayer dielectric layer covering the first buffer layer, the active region, and the gate lamination layer, the interlayer dielectric layer having a plurality of via holes;

a second transparent conductive layer disposed on the interlayer dielectric layer, wherein the second transparent conductive layer covers the active region, and realizes electrical connections of source and drain regions through the via holes;

a planarization layer covering the interlayer dielectric layer and the second transparent conductive layer;

the color film layer disposed on the planarization layer, the color film layer is disposed on the first region;

a second buffer layer covering the color film layer and the planarization;

an anode disposed on the second buffer layer;

a pixel defining layer exposing the anode; and

a light emitting structure covering the pixel defining layer and the anode;

wherein

the active region comprises a first active region and a second active region, the first active region is disposed above the first region and the second active region is disposed above the second region.

2. The OLED display panel according to claim **1**, wherein a projection of the color film layer on a horizontal plane, a

projection of the first region on a horizontal plane, and a projection of the first active region on a horizontal plane overlap.

3. The OLED display panel according to claim **1**, wherein the display panel further comprises a light shielding metal layer between the first transparent conductive layer and the first buffer layer, a projection of the light shielding metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

4. The OLED display panel according to claim **1**, wherein the display panel further comprises a metal layer disposed on the second transparent conductive layer, a projection of the metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

5. The OLED display panel according to claim **4**, wherein material forming the metal layer is a light shielding metal.

6. An organic light emitting diode (OLED) display panel comprising:

a substrate;

a first transparent conductive layer disposed on the substrate, the first transparent conductive layer comprising a first region and a second region; the first region corresponding to a region for forming a color film layer and the second region corresponding to a region for forming a gate lamination layer;

a first buffer layer covering the first transparent conductive layer;

an active region disposed on the first buffer layer;

the gate lamination layer disposed on the active region;

an interlayer dielectric layer covering the first buffer layer, the active region, and the gate lamination layer, the interlayer dielectric layer having a plurality of via holes;

a second transparent conductive layer disposed on the interlayer dielectric layer, wherein the second transparent conductive layer covers the active region, and realizes electrical connections of source and drain regions through the via holes;

a planarization layer covering the interlayer dielectric layer and the second transparent conductive layer;

the color film layer disposed on the planarization layer, the color film layer is disposed on the first region;

a second buffer layer covering the color film layer and the planarization layer;

an anode disposed on the second buffer layer;

a pixel defining layer exposing the anode; and

a light emitting structure covering the pixel defining layer and the anode.

7. The OLED display panel according to claim **6**, wherein the active region comprises a first active region and a second active region, the first active region is disposed above the first region and the second active region is disposed above the second region.

8. The OLED display panel according to claim **6**, wherein a projection of the color film layer disposed on a horizontal plane, a projection of the first region disposed on a horizontal plane, and a projection of the first active region disposed on a horizontal plane overlap.

9. The OLED display panel according to claim **6**, wherein the display panel further comprises a light shielding metal layer between the first transparent conductive layer and the first buffer layer, a projection of the light shielding metal layer disposed on a horizontal plane overlaps with a projection of the second active region disposed on a horizontal plane.

10. The OLED display panel according to claim **6**, wherein the display panel further comprises a metal layer disposed on the second transparent conductive layer, a projection of the metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

11. The OLED display panel according to claim **10**, wherein the material forming the metal layer is a light shielding metal.

12. A method of manufacturing an organic light emitting diode (OLED) display panel, comprising the steps of:

providing a substrate;

forming a first transparent conductive layer disposed on the substrate, wherein the first transparent conductive layer comprises a first region and a second region, the first region is used to form a color film layer, and the second region is used to form a gate lamination layer;

forming a first buffer layer covering the first transparent conductive layer;

forming an active region disposed on the first buffer layer;

forming the gate lamination layer over the active region;

forming an interlayer dielectric layer covering the first buffer layer, the active region, and the gate lamination layer, the interlayer dielectric layer having a plurality of via holes;

forming a second transparent conductive layer disposed on the interlayer dielectric layer, wherein the second transparent conductive layer is disposed above the first region and the second region, and realizes electrical connections of source and drain regions through the via holes;

forming a planarization layer covering the interlayer dielectric layer and the second transparent conductive layer;

forming the color film layer disposed on the planarization layer, the color film layer is disposed over the first region;

forming a second buffer layer covering the color film layer and the planarization layer;

forming an anode disposed on the second buffer layer;

forming a pixel defining layer exposing the anode; and

forming a light emitting structure covering the pixel defining layer and the anode.

13. The method of manufacturing the OLED display panel of claim **12**, wherein the active region comprises a first active region and a second active region, the first active region is disposed above the first region and the second active region is disposed above the second region.

14. The method of manufacturing the OLED display panel of claim **12**, wherein a projection of the color film layer on a horizontal plane, a projection of the first region on a horizontal plane, and a projection of the first active region on a horizontal plane overlap.

15. The method of manufacturing the OLED display panel of claim **12**, wherein after forming the first transparent conductive layer, the method further comprises the following steps:

forming a light shielding metal layer covering the first transparent conductive layer;

patterning the light shielding metal layer, so that its projection on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

16. The method of manufacturing an OLED display panel of claim **12**, wherein the method of patterning the light shielding metal layer and the first transparent conductive layer comprises:

providing a mask having a first pattern for forming the first transparent conductive layer and a second pattern for forming the light shielding metal layer;

forming a photoresist covering the light shielding metal layer and the first transparent conductive layer, the photoresist having a first thickness;

the photoresist is patterned by the mask to form a first photoresist over the first transparent conductive layer and a second photoresist over the light shielding metal layer, the thickness of the first photoresist is less than the thickness of the second photoresist;

the light shielding metal layer and the first transparent conductive layer are patterned by using the first photoresist and the second photoresist as a mask.

17. The method of manufacturing the OLED display panel according to claim **16**, wherein, the first pattern and the second pattern of the mask have different transmittances, and the transmittance of the first pattern is smaller than the transmittance of the second pattern.

18. The method of manufacturing the OLED display panel according to claim **12**, wherein, after forming the second transparent conductive layer, the method further comprises the steps of:

forming a metal layer over the second transparent conductive layer, a projection of the metal layer on a horizontal plane overlaps with a projection of the second active region on a horizontal plane.

19. The method of manufacturing the OLED display panel according to claim **18**, wherein, the material forming the metal layer is a light shielding metal.

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专利名称(译)	有机发光二极管显示器及其制造方法		
公开(公告)号	US20200227499A1	公开(公告)日	2020-07-16
申请号	US16/492156	申请日	2019-04-01
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
[标]发明人	TANG JIA IM JANGSOON		
发明人	TANG, JIA IM, JANGSOON		
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摘要(译)

提供了一种有机发光二极管(OLED)显示面板及其制造方法。 显示面板包括:基板,其包括彩色膜层和第一透明导电层;以及第二基板。 第一透明导电层包括第一区域和第二区域。 有源区包括第一有源区和第二有源区,所述第一有源区位于所述第一区的上方,所述第二有源区位于所述第二区的上方。 栅极叠层,层间介电层,第二透明导电层,平坦化层,阳极和设置在第二有源区上的像素限定层。